AMENDMENT TO THE CLAIMS:

Claims 1-8. (Cancelled)

9. (Currently amended) A photo mask set comprising:

a first photo mask in which a first intended pattern and a first alignment mark are defined; and

a second photo mask in which a second intended pattern to overlay with the first intended pattern is defined,

wherein a part of the second intended pattern, and the first alignment mark have a substantially same ~~line width~~ width of a pattern and line spacing.

10. (Cancelled)

11. (Currently amended) The photo mask set claim 9, wherein the both width of pattern and ~~a spaee~~ line spacing in the first alignment ~~mask~~ mark is equal to ~~the smallest width~~ a part ~~of the second intended pattern~~ having the smallest width of a pattern and line spacing of the second intended pattern.

12. – 15. (Cancelled)

16. Currently amended) An alignment method comprising the steps of:

forming a first on-wafer intended pattern, and a first on-wafer alignment mark, ~~and a second on-wafer alignment mark~~ on a substrate by exposure using a first photo mask in which a first intended pattern, and a first alignment mark, ~~and a second alignment mark~~ are defined;

calculating a correction value from ~~a positional relationship~~ a declination between ~~the first on-wafer alignment mark and the second on-wafer alignment mark formed on the substrate~~ the designed first alignment mark and the first on-wafer alignment mark formed on the substrate by exposure; and

correcting the declination ~~differences of overlay by the correction value~~ when ~~in overlaying~~ a second intended pattern [[in]] having a second photo mask overlays with the first on-wafer intended pattern,

wherein the first alignment mark in the first photo mask, and the second intended pattern in the second photo mask has a substantially same [[line]] width of a pattern and line spacing ~~as the second alignment mark in the first photo mask~~.

17. (Currently amended) The alignment method of claim 16, wherein the [[line]] both width of a pattern and a space in the second alignment mark are equal to a part having the smallest width of a pattern and a space in the second intended pattern.

18. – 19. (Cancelled)

20. (New) The photo mask set claim 9:

wherein the first photo mask in which a first intended pattern, a first alignment mark, and a second alignment mark are defined; and

wherein the second alignment mark has substantially the same width of a pattern and line spacing as at least part of the first intended pattern.

21. (New) The photo mask set claim 9, wherein the width of a pattern and a space in the first intended pattern is larger than the width of a pattern and a space in the second intended pattern.

22. (New) The photo mask set claim 9, wherein the first intended pattern defines an isolation region, and the second intended pattern defines a gate electrode.

23. (New) An alignment method according to claim 16:

wherein the first photo mask in which a first intended pattern, a first alignment mark, and a second alignment mark are defined; and

wherein the second alignment mark has substantially the same width of a pattern and line spacing as at least a part of the first intended pattern..

24. (New) An alignment method according to claim 23:

forming a first on-wafer intended pattern, a first on-wafer alignment mark, and a second on-wafer alignment mark on a substrate by exposure using a first photo mask in which the first intended pattern, the first alignment mark, and the second alignment mark are defined;

calculating a correction value from a declination between a designed distance between the first alignment mark and the second alignment mark, and a real distance between the first on-wafer alignment mark and the second on-wafer alignment mark formed on the substrate by exposure; and

correcting the declination between the designed distance and the real distance when a second intended pattern having a second photo mask overlays with the first on-wafer intended pattern.

25. (New) An alignment method according to claim 16, wherein the width of a pattern and line spacing in the first intended pattern is larger than the width of a pattern and line spacing of the second intended pattern.

26. (New) An alignment method according to claim 16, wherein the first intended pattern defines an isolation region, and the second intended pattern defines a gate electrode.